REMARKS

Applicants respectfully request further examination and reconsideration in view of the above amendments. Claims 15-30 remain pending in the case. Claims 15-30 are rejected. Claim 16 is amended herein. No new matter has been added.

35 U.S.C. §103(a)

Claims 15-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent 6,477,084 by Eitan, hereinafter the "Eitan" reference, in view of United States Patent 5,879,990 by Dormans, et al., hereinafter the "Dormans" reference. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 15-30 are not anticipated nor rendered obvious by Eitan in view of Dormans.

Independent Claim 16 recites (emphasis added):

> A process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:
>
> forming a gate above said channel of said substrate, wherein said gate comprises a polysilicon layer;
>
> <u>forming a bitline subsequent to said forming said gate comprising said polysilicon layer</u>; and
>
> siliciding said bitline.

Claims 15 and 17-30 that depend from independent Claim 16 provide further recitations of the limitations of the present invention as claimed.

The combination of Eitan and Dormans does not teach a method for fabricating a memory cell comprising forming a gate above said channel of said substrate, wherein said gate comprises a polysilicon layer, prior to forming a bitline, as claimed. Eitan and the claimed embodiments of the claimed invention are very different. Applicants understand Eitan to teach a NROM cell with a pocket implant self-aligned to at least one bit line junction. As pointed out by the Examiner, Eitan does not teach siliciding a bitline.

In particular, Eitan teaches forming a bitline prior to depositing the polysilicon on the gates. Applicants respectfully direct Examiner to Figure 7B of Eitan. Bit lines 104 are implanted between the columns of the bit line mask 168 through the oxide layer 160 (col. 8, lines 26-38). Subsequent to the bit line formation, polysilicon gates are deposited. In particular, Eitan states that "[t]he final step is the deposition of the polysilicon gates ..., in accordance with standard deposition techniques" (col. 10, lines 16-18 and Figure 7E).

In contrast, embodiments of the claimed invention are directed towards "forming a bitline subsequent to said forming said gate comprising said polysilicon layer" as recited in Claim 16. In particular, as described in the current specification, a polysilicon layer is deposited as shown at step 212 of Figure 2 of the present invention (page 5, lines 5-11).

Subsequently, the bitline is formed, as shown at step 220 of Figure 2 (page 6, lines 10-22).

Applicants respectfully assert that Eitan teaches a process of manufacturing a NROM cell wherein a bitline is formed prior to depositing the polysilicon on the gates. Therefore, Applicant respectfully asserts that Eitan not only does not suggest a process of fabricating a memory cell wherein polysilicon is deposited prior to bitline formation, as claimed, but rather <u>teaches away from</u> such a combination.

Moreover, the combination of Eitan and Dormans fails to teach or suggest this claim limitation because Dormans does not overcome the shortcomings of Eitan. Dormans, alone or in combination with Eitan, does not show or suggest a process of fabricating a memory cell comprising forming a gate above said channel of the substrate, wherein the gate comprises a polysilicon layer, prior to forming a bitline, as claimed. As described above, Eitan teaches manufacturing a NROM cell wherein a bitline is formed prior to depositing the polysilicon on the gates.

Applicants understand Dormans to teach a semiconductor device having an embedded non-volatile memory. Dormans does not teach, show or suggest fabricating a memory cell, as claimed. In particular, Dormans does not show or suggest a process of

fabricating a memory cell comprising forming a gate above said channel of the substrate, wherein the gate comprises a polysilicon layer, prior to forming a bitline, as claimed.

In view of the claim limitation of "forming a bitline subsequent to said forming said gate comprising said polysilicon layer" not being shown or suggested in Dormans, in combination with the above arguments, Applicants respectfully submit that independent Claim 16 overcome the cited references and are therefore allowable over the combination of Eitan and Dormans.

Furthermore, Applicants respectfully assert that the combination of Eitan and Dormans is inoperative for its intended purpose. In order to combine references, the references cannot be rendered unusable for their intended purpose. In particular, the NROM cell of Eitan comprises a thermally grown oxide layer over the bit lines. Eitan specifically recites that "[a] gate oxide layer is now <u>thermally</u> grown over the entire array using standard oxidation techniques" (col. 9, lines 52-54, emphasis added). "In the array, the oxidation step causes oxide, labeled 178 in Figure 7F, to grow over bit lines 104" (col. 9, lines 56-57).

In contrast, embodiments of the present invention are directed towards a process for fabricating a memory cell comprising "siliciding said bitline," as claimed. In particular, as described in the present specification at page 7, lines 4-8, an oxide <u>deposition</u> is made

on the bitline regions and the gate electrodes. The oxide deposition occurs subsequent to the silicidation of the bitline, as shown in Figure 2 at steps 226 and 228.

Applicants understand Dormans to form titanium silicide on the poly gates and the source and drain zones of the transistors under the influence of heating (col. 5, lines 24-26). Applicants respectfully assert that it is not possible to thermally grow a pure oxide on titanium silicide. In particular, it is not possible to prevent the titanium from mixing with the oxide. By thermally growing an oxide over titanium silicide, the titanium would introduce impurities into the oxide. Introducing impurities into the oxide markedly and unpredictably changes the dielectric properties of the oxide. For semiconductor devices, in particular flash memory cells, it is necessary to know the dielectric properties of the oxide to ensure proper and consistent functioning. One skilled in the art would know that introducing impurities into the oxide would change the dielectric properties of the oxide and is not desirable.

As stated in Dormans (col. 5, lines 24-27), the titanium does not change into titanium silicide on the field oxide. Moreover, a pure oxide cannot be thermally grown over silicide, as the silicide would be mixed with the oxide, altering the material properties of the silicide and the oxide. Rather, a mixed oxide film of some nature would result. As described above, it is necessary to avoid contaminating the oxide with impurities to ensure proper functioning of the memory cell.

Applicants respectfully assert that the silicide as described in Dormans cannot be placed on the bitline of Eitan, as the bitline of Eitan comprises a thermally grown oxide. Therefore, Applicants respectfully assert that the combination of Eitan and Dormans not only does not suggest a process of fabricating a memory cell comprising siliciding a bitline, as claimed, but rather such a combination is unusable for its intended purpose.

With reference to U.S. Patent Application 6,156,644 by Ko et al., hereinafter referred to as the "Ko" reference, it is suggested that a rapid thermal oxide dielectric film of silicon dioxide may be formed on a gate line of tungsten oxide (col. 7, lines 13-18). As described above, thermally growing an oxide over a silicide alters the dielectric properties of both the oxide and silicide. In particular, thermally growing an oxide over titanium silicide will result in the titanium being incorporated into the oxide. Furthermore, as stated in Ko, when the thermal oxide is formed, "the contact resistance between the bit line and the gate is increase without heat treatment" (col. 7, lines 16-18).

Applicants understand Ko to teach that forming a thermal oxide over tungsten silicide results in adversely affecting the material properties of the interconnect, and therefore is undesirable. Therefore, Applicants respectfully assert that Ko further establishes that the combination Eitan and Dormans is unusable for its intended purpose.

Applicants respectfully assert that nowhere does the combination of Eitan and Dormans teach, disclose or suggest the present invention as recited in independent Claim 16, and that this claim is thus in a condition for allowance. Therefore, Applicants respectfully submit that the combination of Eitan and Dormans also does not show or suggest the additional claimed features of the present invention as recited in Claims 15 and 17-30 which depend from independent Claim 16. Therefore, Applicants respectfully submit that Claims 15 and 17-30 overcome the Examiner's basis for rejection under 35 U.S.C. § 103(a) as these claims are dependent on an allowable base claim.

CONCLUSION

Based on the arguments presented above, Applicants respectfully assert that Claims 15-30 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these Claims.

Applicants have reviewed the following references which were cited but not relied upon and do not find these reference to show or suggest the present claimed invention: U.S. 6,211,548, U.S. 6,346,442, U.S. 5,250,846, U.S. 6,518,124, U.S. 6,174758 and U.S. 2002/0142546.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge our deposit account No. 23-0085 for any unpaid fees.

Respectfully submitted,
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